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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,254	12/20/2005	Raymond J.E. Huetting	GB030096US1	5647
65913	7590	08/17/2007	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			KUO, WENSING W	
			ART UNIT	PAPER NUMBER
			2809	
			NOTIFICATION DATE	DELIVERY MODE
			08/17/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

[ip.department.us@nxp.com](mailto:ip.department.us@nxp.com)

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/562,254	HUETING, RAYMOND J.E.	
	Examiner	Art Unit	
	W. Wendy Kuo	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 20 December 2005.

2a) This action is FINAL.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-10 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 20 December 2005 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 20 Dec. 2005.

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.

5) Notice of Informal Patent Application

6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Objections***

1. Claims 1, 5, and 6 objected to because of the following informalities:
  - Regarding claim 1, lines 17-18 should be corrected to fix the typographical errors
  - Regarding claim 5, line 3 should be corrected to fix the typographical error
  - Regarding claim 6, line 3 should be corrected to fix the typographical error

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
3. Claims 1-3 and 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huetting et al., US 6,515,348 in view of Dennen, US 6,555,872.
4. With respect to claim 1, Huetting et al. teach in Figure 9 a semiconductor device having opposed first and second major surfaces, comprising:
  - A body region (3, 3a) at the first major surface;
  - At least one cell having longitudinally spaced source 5 and drain 6 implantations

extending into the body region (3, 3a) from the first major surface, the source and drain implantations being spaced away from the substrate 2 by part of the body region and defining a channel part of the body region between the source and drain implantations; and

At least one insulated gate trench (4 Figure 1) extending longitudinally from the source implantation 5 to the drain implantation 6 through the body region (3, 3a), the insulated gate trench including a gate conductor 7b insulated from the source and drain implantations and the body region by a gate dielectric 7a along the side (4c, 4d) and end (4a, 4b) walls and the base 4e of the trench, the source and drain implantations extending along part of the side walls of the trench.

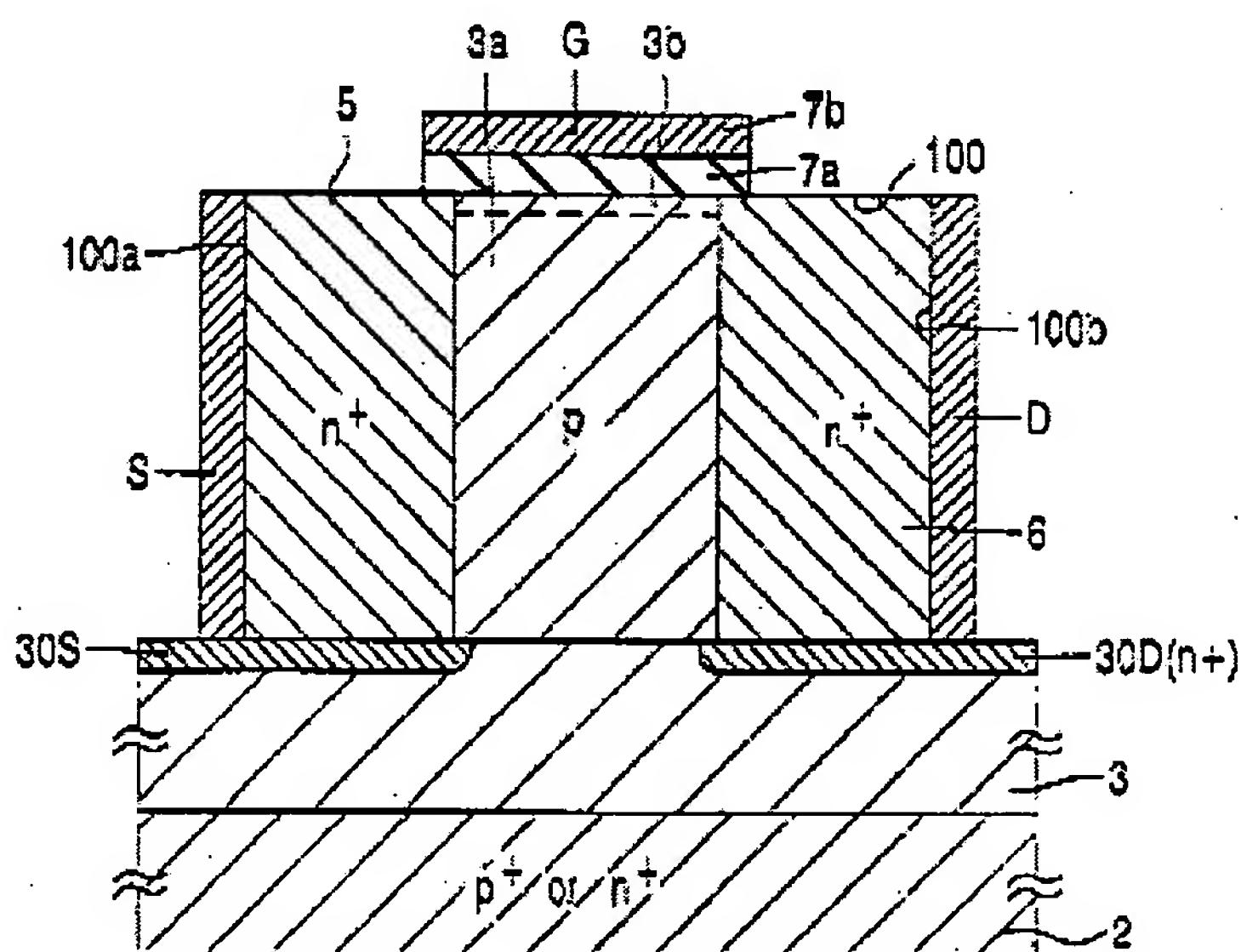


FIG. 9

Huetting et al. fail to teach that the source and drain implantations include conductive shallow contact regions at the first major surface extending vertically into the

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body region to a depth of no more than 35% the depth of the trench. Dennen teaches in Figure 9 that the source and drain implantations include conductive shallow contact regions (123, 124) at the first major surface extending vertically into the body for the benefit of maximizing the breakdown voltage of trench gate Fermi-FET transistors (column 26, lines 35-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Huetting et al. with the conductive shallow contact regions of Dennen for the benefit of maximizing the breakdown voltage of trench gate Fermi-FET transistors.

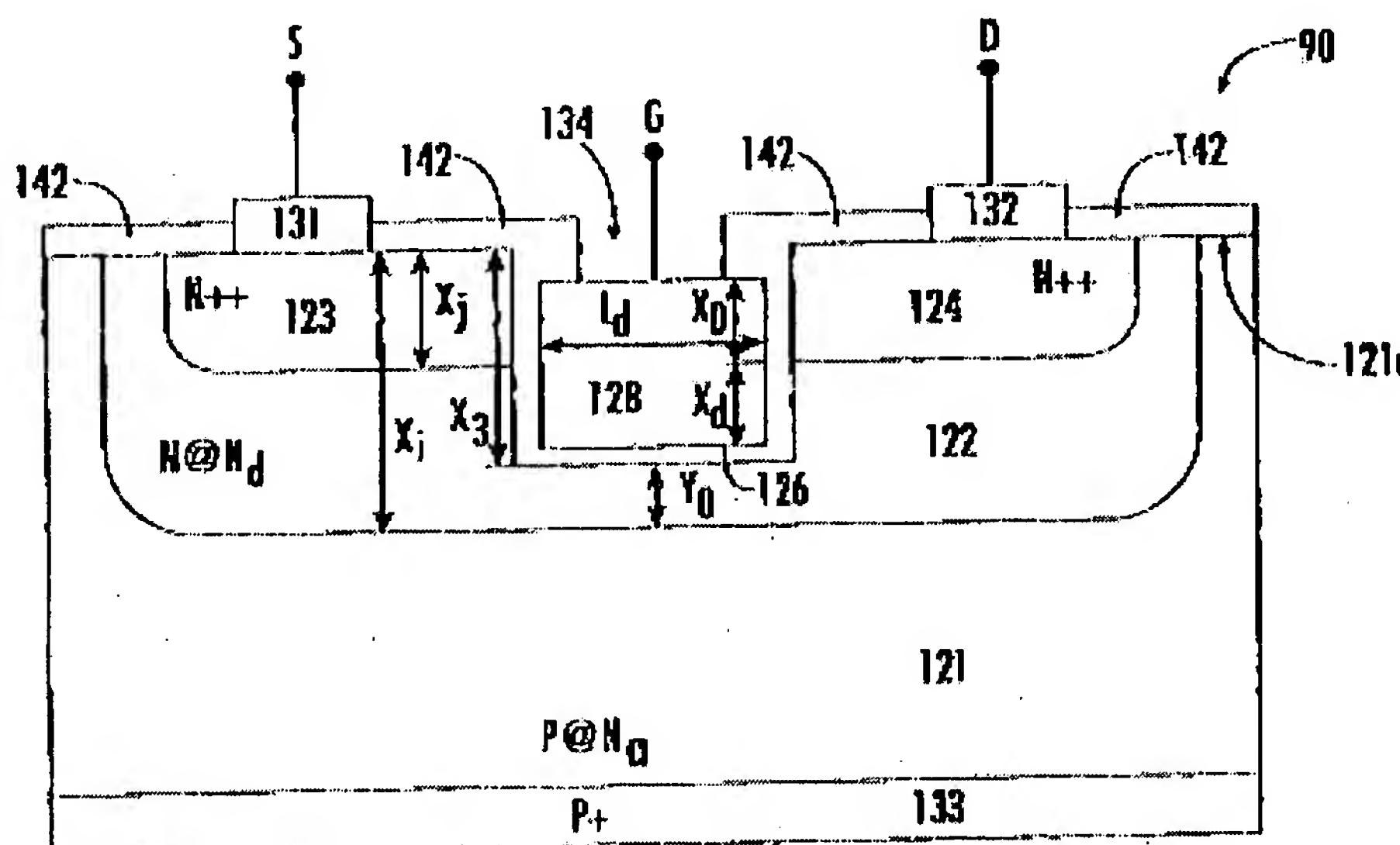


FIG. 9.

Huetting et al. in view of Dennen remains as applied above.

Huetting et al. in view of Dennen fail to teach that the conductive shallow contact regions at the first major surface extending vertically into the body region extend to a depth of no more than 35% the depth of the trench. However, Dennen teaches that it is

preferable to make the source and drain regions shallow enough to maximize the breakdown voltage of the trench gate Fermi-FET transistor (column 26, lines 35-41).

Dennen further teaches that the values of implants and depths can be arrived at in simulation (column 27, lines 2-4). "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Since the applicant has not established the criticality (see next paragraph) of the ratio of the depth of the shallow contact regions to the depth of the trench, it would have been obvious to one of ordinary skill in the art to use these values in the device of Hueting et al. in view of Dennen.

#### CRITICALITY

The specification contains no disclosure of either the critical nature of the claimed implant to trench depth ratio or any unexpected results arising therefrom. Where the patentability is said to be based upon particular chosen dimensions of upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

5. With respect to claims 2, 3, and 5-10, Hueting et al. in view of Dennen remains as applied to claim 1 above.

6. With respect to claim 2, Dennen further teaches in Figure 9 that the body region is of a first conductivity type (P@Na) and the shallow contact regions are of a second conductivity type (N++) opposite to the first conductivity type.

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7. With respect to claim 3, Dennen further teaches each of the source and drain implantations further comprises a lower doped region 122 of lower doping (N@Nd) than the shallow contact region (N++).
8. With respect to claim 5, Huetting et al. further teach in Figure 12 that the semiconductor device comprises as plurality of cells (FD) laterally spaced across the first major surface.
9. With respect to claim 6, Huetting et al. further teach that the gate trenches alternate with cells laterally across the surface (column 8, lines 26-31).
10. With respect to claim 7, Huetting et al. further teach that each cell has a gate trench laterally within the confines of the cell (column 8, lines 49-51).
11. With respect to claim 8, Dennen further teaches that the lower doped region 122 of lower doping than the shallow contact region extends vertically below the shallow contact region to a depth at least 80% of the depth of the trench.
12. With respect to claim 9, Dennen further teaches that the source and drain implantations consist exclusively of the shallow contact region (Figure 4).
13. With respect to claim 10, Huetting et al. further teach that the semiconductor device is on a conductive substrate 2 of first conductivity type (P+).
14. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huetting et al., US 6,515,348 in view of Dennen, US 6,555,872 as applied to claim 3 above, and further in view of Huetting et al., US 6,534,823.

Dennen further teaches in Figure 9 that the source implantation includes a higher

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doped shallow source contact region 123 and a lower doped source drift region 122 between the higher doped source contact region and the body 121; the drain implantation includes a higher doped shallow drain contact region 124 and a lower doped drain drift region 122 between the higher doped drain contact region and the body 121.

Huetting et al. in view of Dennen fail to teach that the insulated gate trench includes potential plate regions extending longitudinally on either side of a central region, the potential plate regions being adjacent to the source and drain drift regions respectively, and the central region being adjacent to the body; and the thickness of the gate dielectric sidewalls of the insulated gate trench is greater in the potential plate regions of the insulated gate than the central region. Huetting et al. (US 6,534,823) teach in Figure 1 that the insulated gate trench 80 includes potential plate regions 71 extending longitudinally on either side of a central region 70 (field plate region 71 is depicted as extending either to the right or to the left of gate structure 70), the potential plate regions being adjacent to the source and drain drift regions 50 respectively, and the central region 70 being adjacent to the body 6; and the thickness of the gate dielectric sidewalls of the insulated gate trench 80 is greater in the potential plate regions 71a of the insulated gate than the central region 70a for the benefit of providing a lateral field effect device having a trench gate structure with a low on-resistance and good reverse voltage withstand characteristics (column 1, lines 42-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Huetting et al. in view of Dennen with the

potential plate regions of Huetting et al. (US 6,534,823) for the benefit of providing a lateral field effect device having a trench gate structure with a low on-resistance and good reverse voltage withstand characteristics.

### ***Conclusion***

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Easter et al., US 4,839,309 disclose a method of fabricating a dielectrically isolated structure.

Gilbert et al., US 5,349,224 disclose an integrable MOS and IGBT device having a trench gate structure.

Redwine et al., US 5,349,225 disclose a transistor device formed in a semiconductor layer with a lightly doped portion and a deep portion.

Miyamoto et al., US 5,359,221 disclose a semiconductor device with source and drain regions formed in a first region of low concentration, and a second region with doping concentration higher than that of the first region is formed around the first region.

Gardner et al., US 6,201,278 disclose an IGFET with a gate electrode and insulative spacers in a trench.

Fujishima et al., US 6,316,807 disclose a high-voltage and low on-resistance semiconductor device that incorporates a trench structure that provides improved switching characteristics.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. Wendy Kuo whose telephone number is (571) 270-1859. The examiner can normally be reached Monday through Friday 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Angela Ortiz can be reached at (571) 272-1206. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*Wensing Wendy K*

WWK

*L.A.J.*  
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PRIMARY EXAMINER